REMARKS

Rejection of Claims 1, 2, 7, 8 and 13 Under 35 U.S.C. §102(b) based on U.S. Patent No. 5,329,139 (*Sanada*).

The semiconductor apparatus of amended claim 1 includes a plurality of device elements formed on a surface of a semiconductor substrate. Each device element has a diffusion region. The semiconductor apparatus also includes a multi-layer wiring configuration electrically connecting at least two of the diffusion regions. A first one of the plurality of wiring layers is divided into a first wiring region for providing wiring in a first direction and a second wiring region for providing wiring in a second direction.

As is well established, anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.[1] Because the cited reference is not believed to show first and second writing regions, as described in claim 1, this rejection is traversed.

Sanada is directed to a semiconductor integrated circuit device that can be subject to non-destructive analysis, such as a laser probe for generating electron hole pairs. The rejection of claim 1 refers to an inverter circuit of *Sanada* that includes two wiring layers. One wiring layer has a wiring that extends in a first direction and another that extends in a second direction.[2] However, such a showing is not believed to show Applicant's claim 1 limitations.

Applicant's claim 1 recites first and second regions of a semiconductor apparatus for providing wiring in different directions, and not first and second wirings of a same layer that extend in different directions. That is, the rejection has pointed to particular wirings, and not semiconductor device regions for providing wiring directions.

Thus, because the rejection does not show particular regions for providing wiring in different directions, this ground for rejection is traversed.

The rejection of Claims 7, 8, and 13 will now be addressed.

The semiconductor apparatus of amended claim 7 includes a plurality of functional circuit blocks, each functional circuit block including a plurality of device elements, a first wiring

[1] See Lindemann Maschinenefabrick GmbH v. American Hoist & Derrick Col., 221 USPQ 481, 485 (Fed. Cir. 1984).

region and a second wiring region. Also included is a multi-layer wiring configuration electrically connecting predetermined ones of the device elements. A first one of the plurality of wiring layers is divided into a first wiring region for providing wiring in a first direction and a second wiring region for providing wiring in a second direction.

Applicant incorporates by reference herein the comments set forth above for claim 1. Namely, that the rejection shows wiring and not wiring regions for providing wiring in different directions.

The present claims 1-13 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

Darl Walker January 3, 2003

Darryl G. Walker
Attorney
Reg. No. 43,232

Darryl G. Walker
Attorney/Agent
300 South First Street
Suite 235
San Jose, CA 95113
Tel. 1-408-289-5314

[2] See *Sanada*, FIG. 7, which shows input signal line 34c and output signal line 34d.